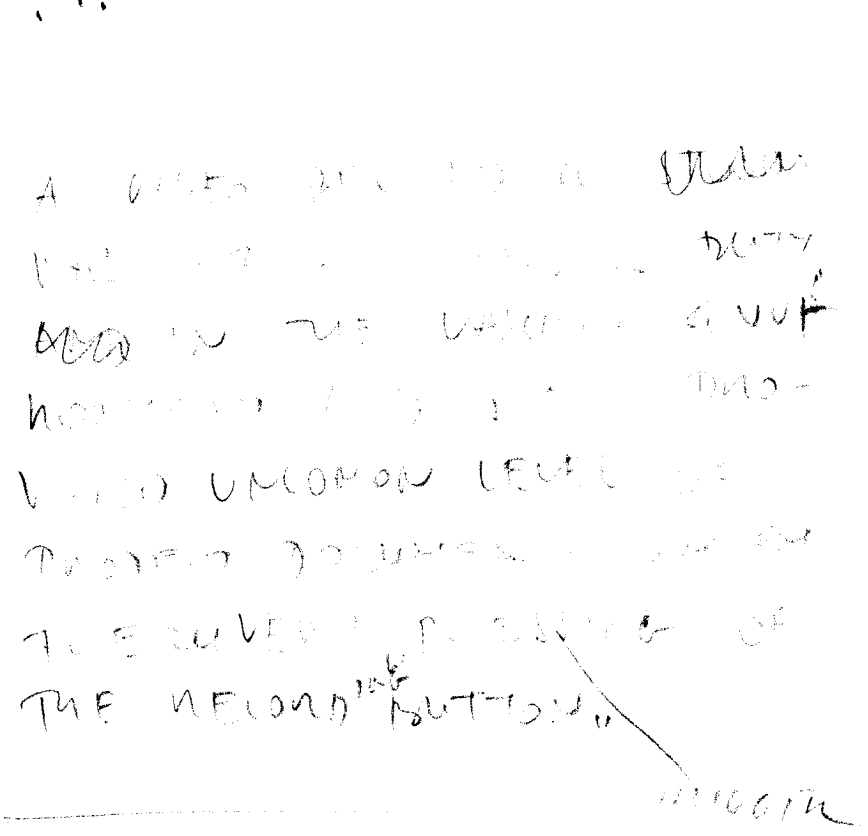
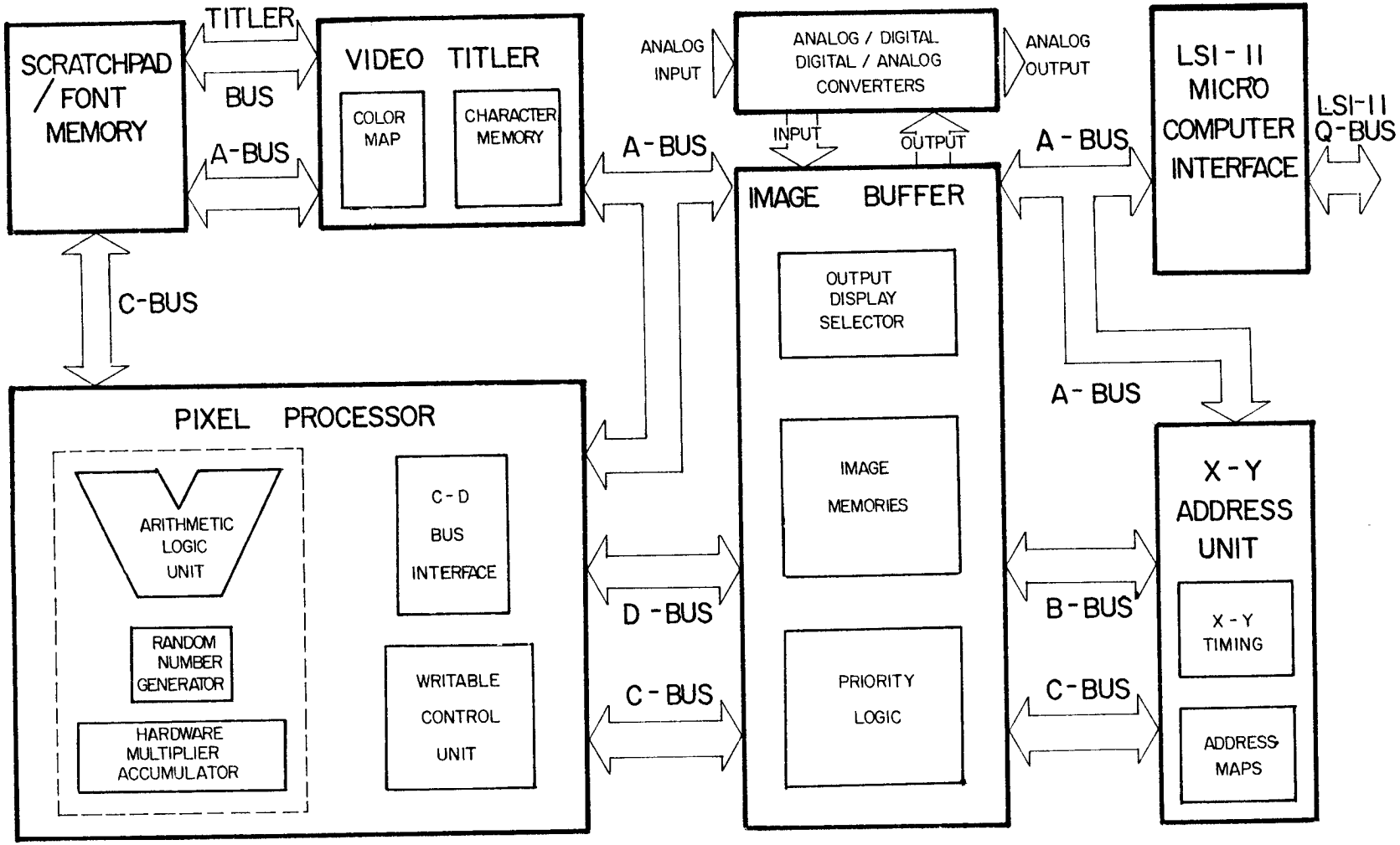
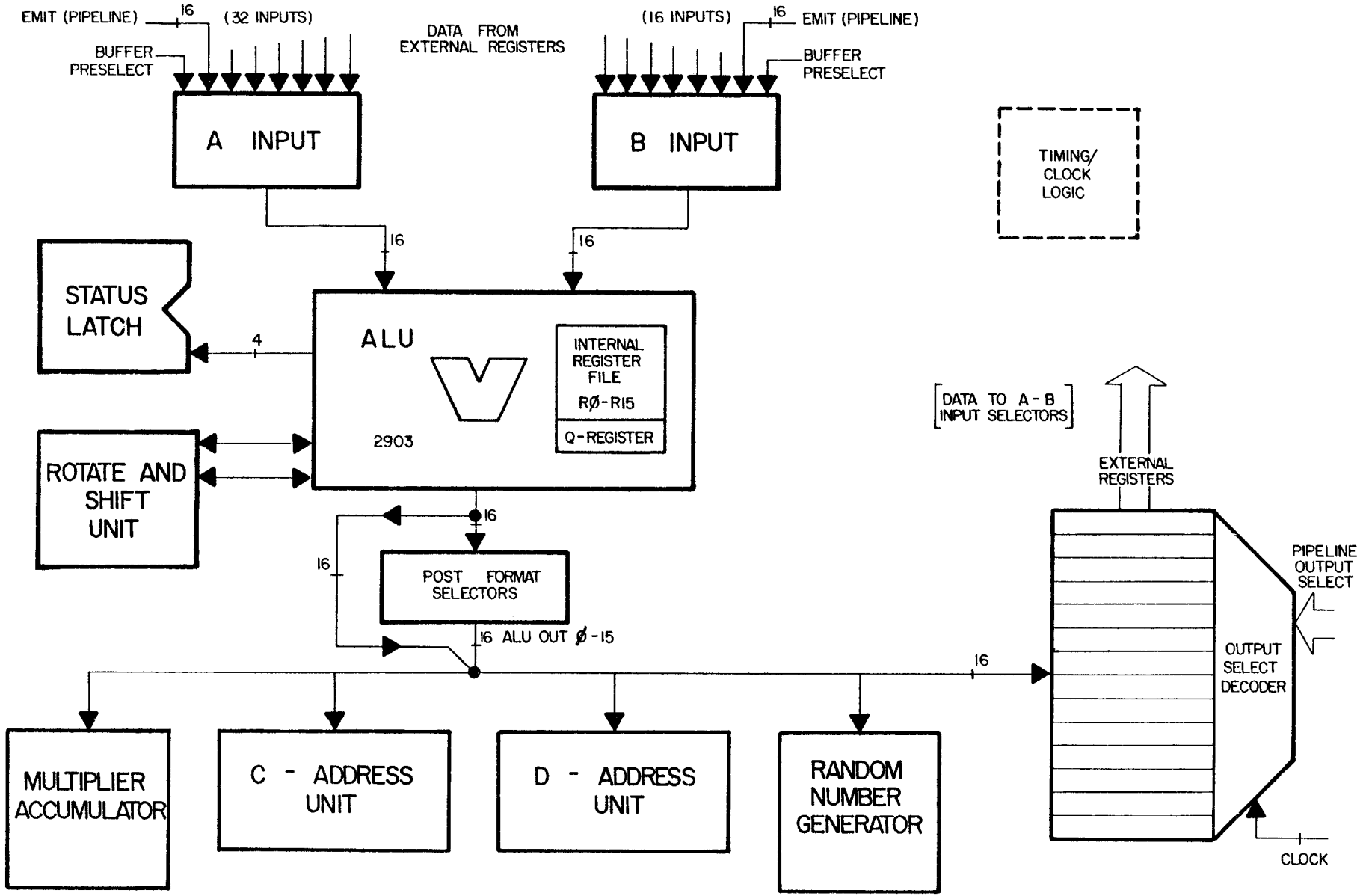


RANDOM ACCESS MEMORY
RAM SOUND
BEFORE STANDARD TEXT
NEWLY
PATTERN FOR
GUI INSTRUMENT

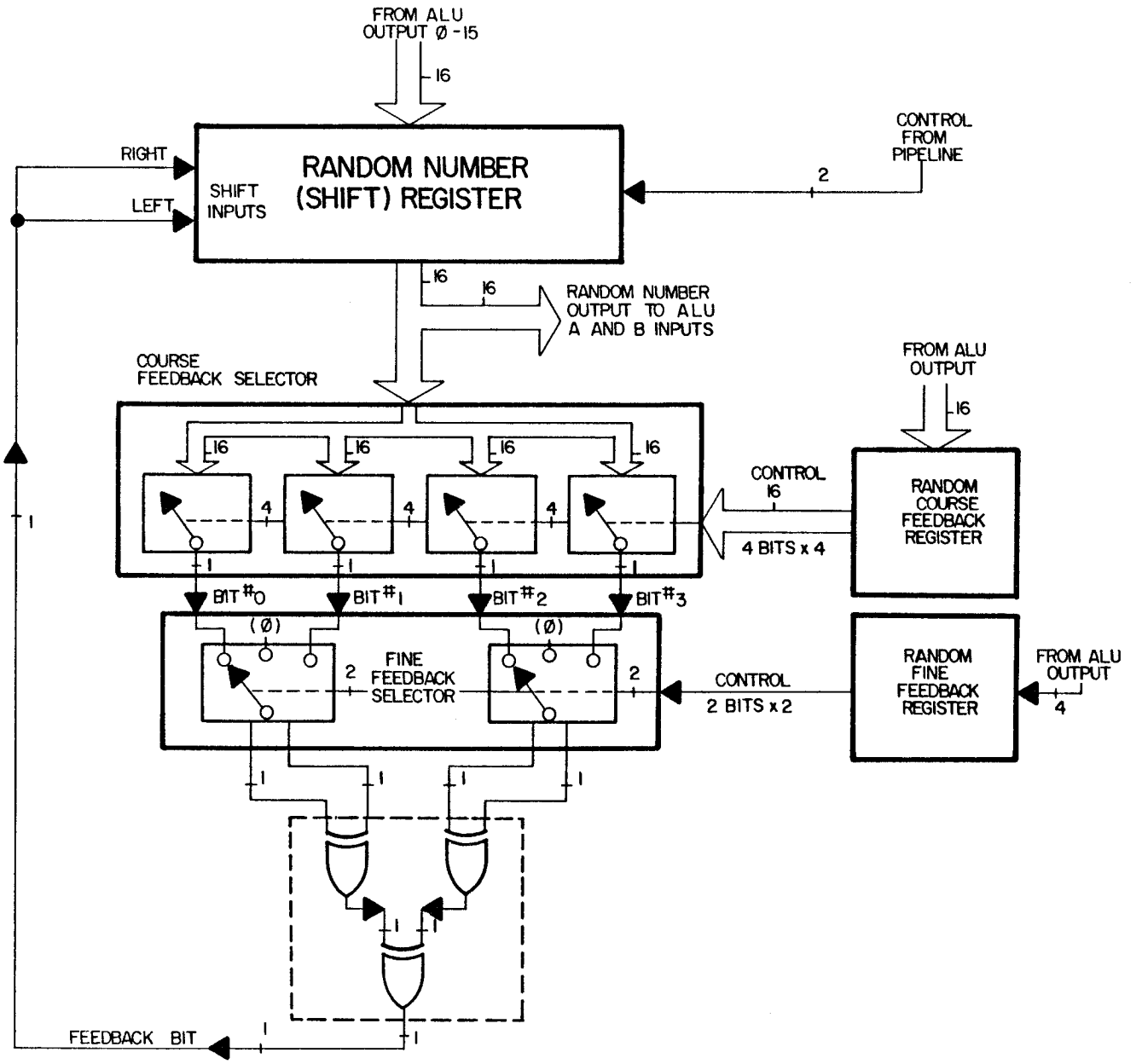
BLOCK OVERVIEW



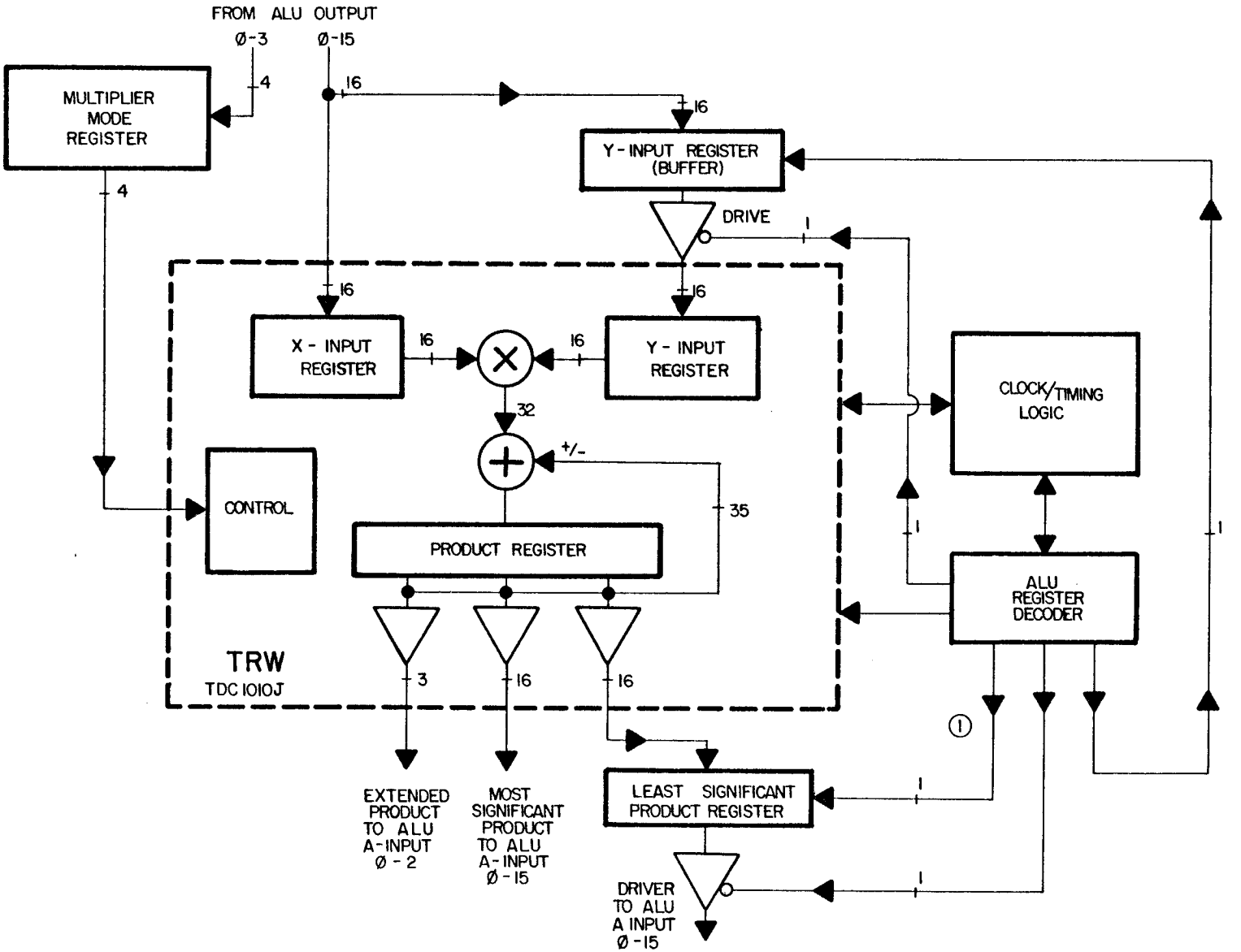
ARITHMETIC LOGIC UNIT - REGISTER SECTION



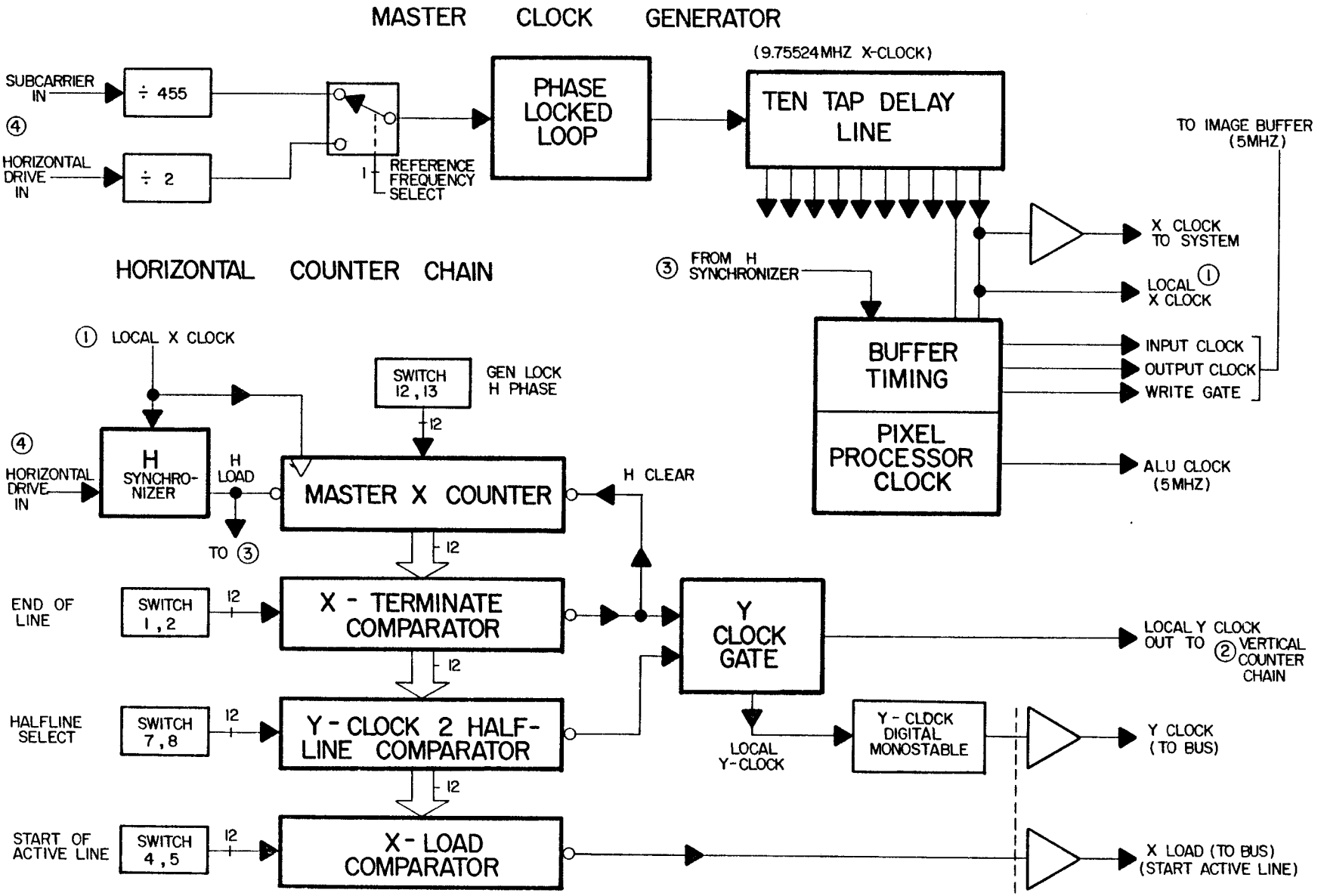
HARDWARE RANDOM NUMBER GENERATOR



HARDWARE MULTIPLIER - ACCUMULATOR

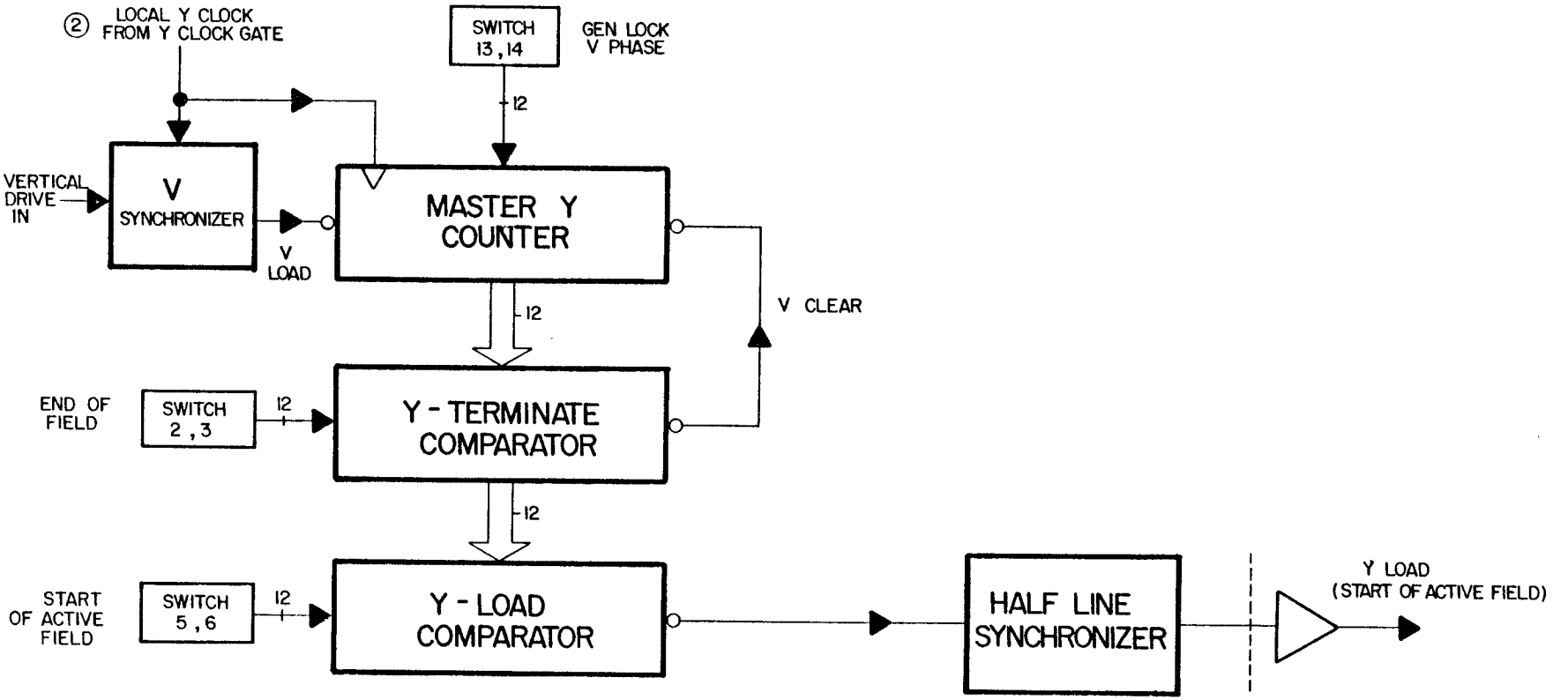


MASTER X-Y TIMING - GENERATOR LOCK



MASTER X-Y TIMING - GENERATOR LOCK

VERTICAL COUNTER CHAIN



ANALOG TO DIGITAL CONVERTERS (HIGH SPEED - VIDEO)

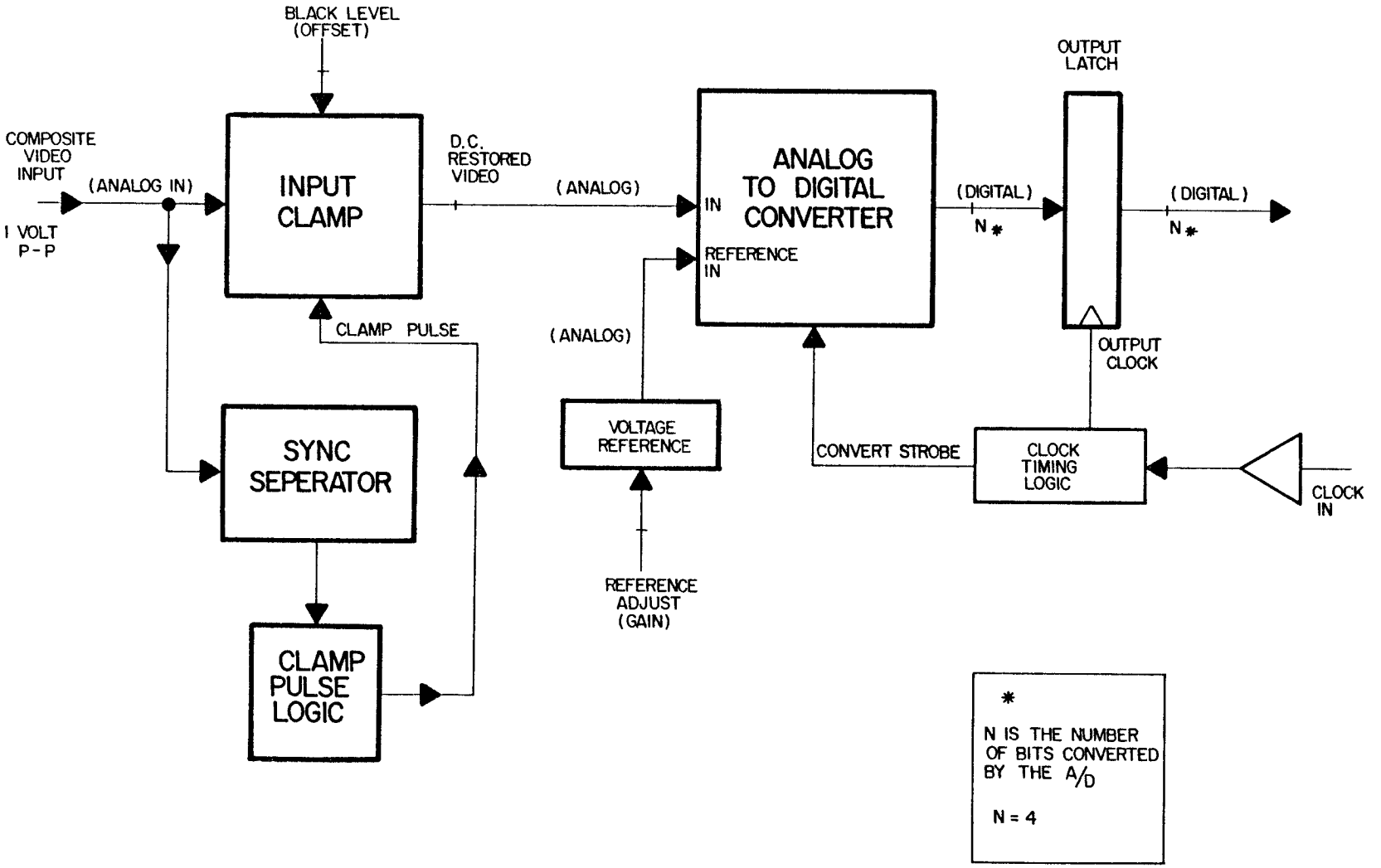
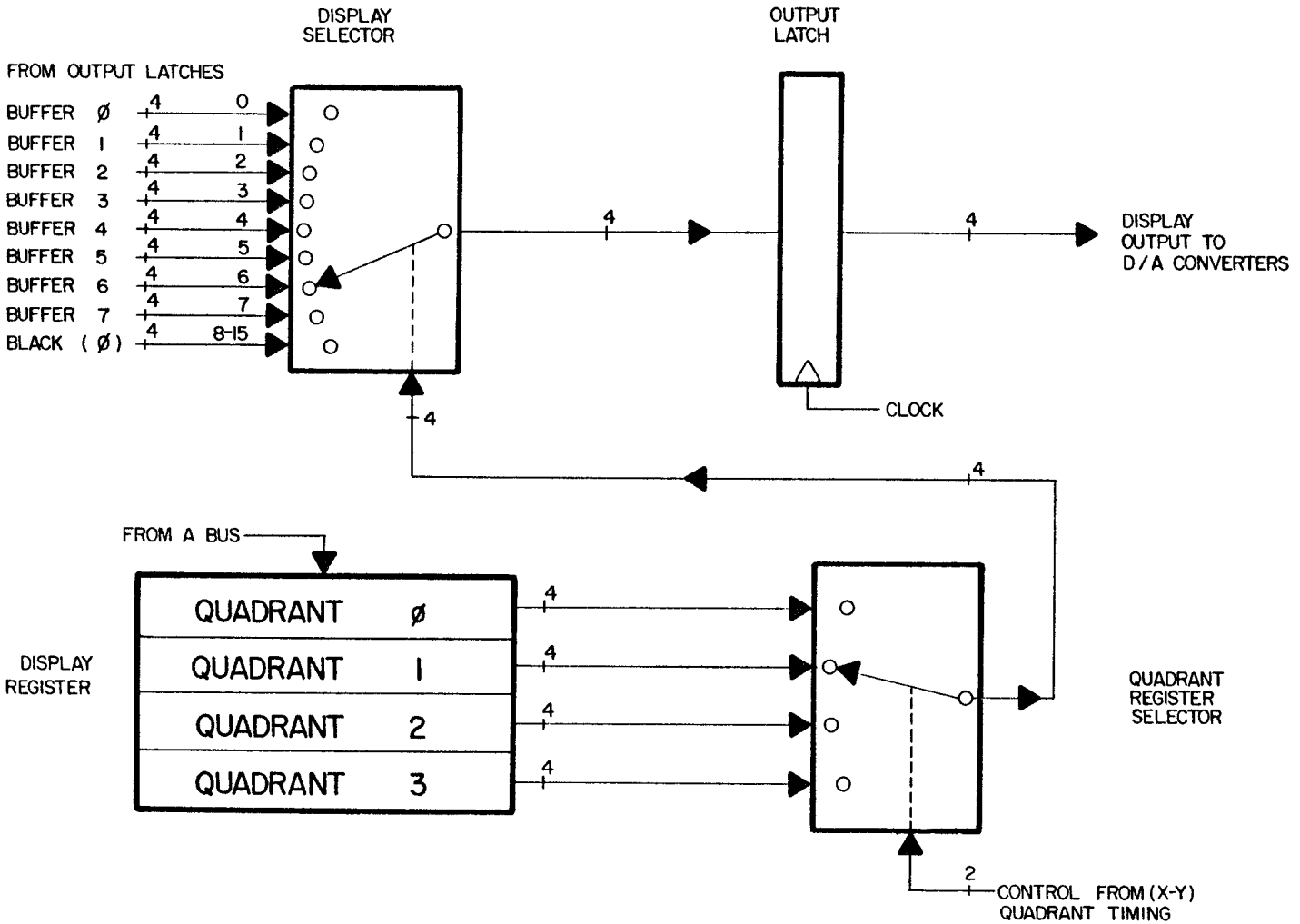
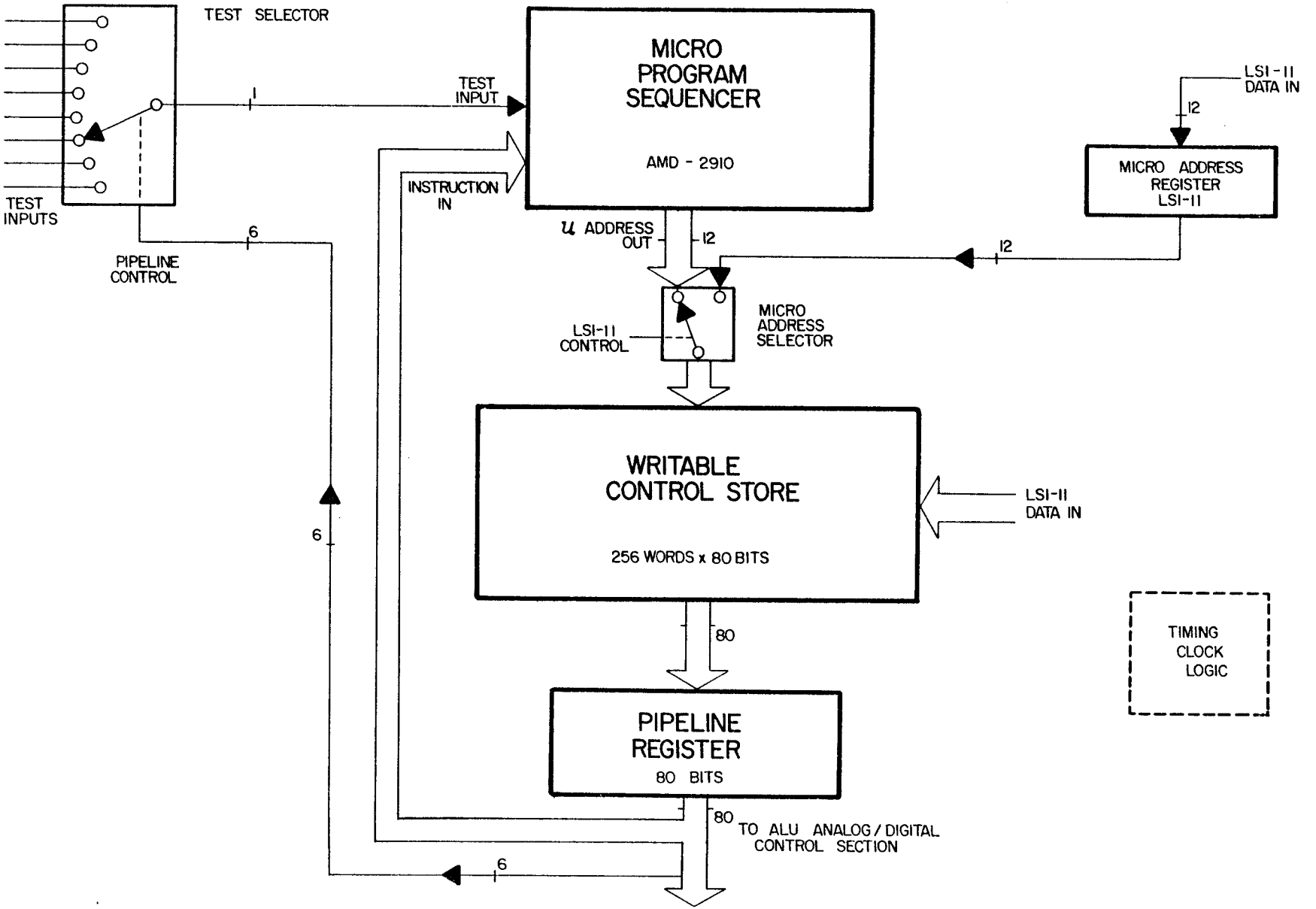


IMAGE OUTPUT DISPLAY SELECTOR

(1 OF 4)



SEQUENCER - CONTROL UNIT



X-Y ADDRESS UNIT

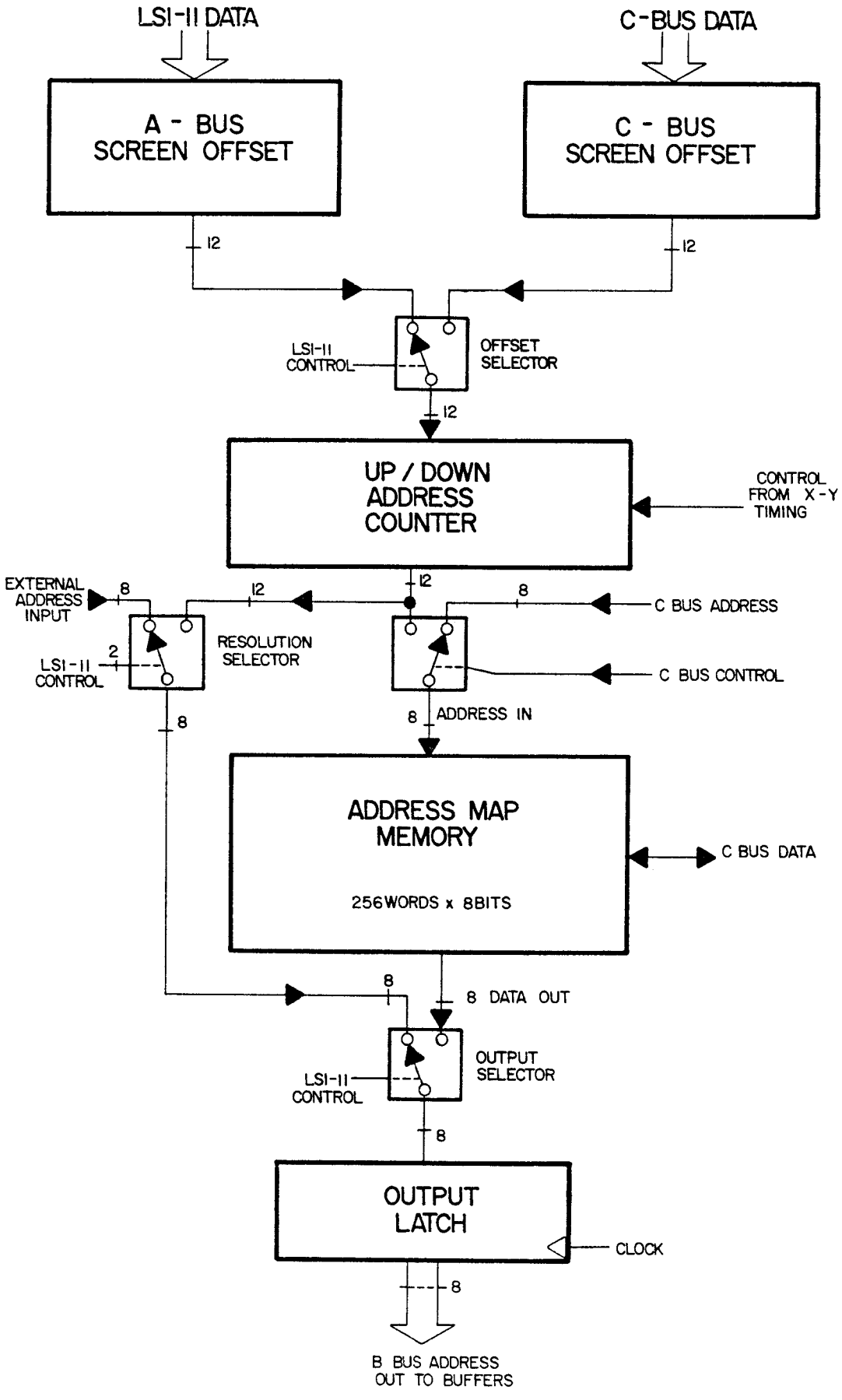
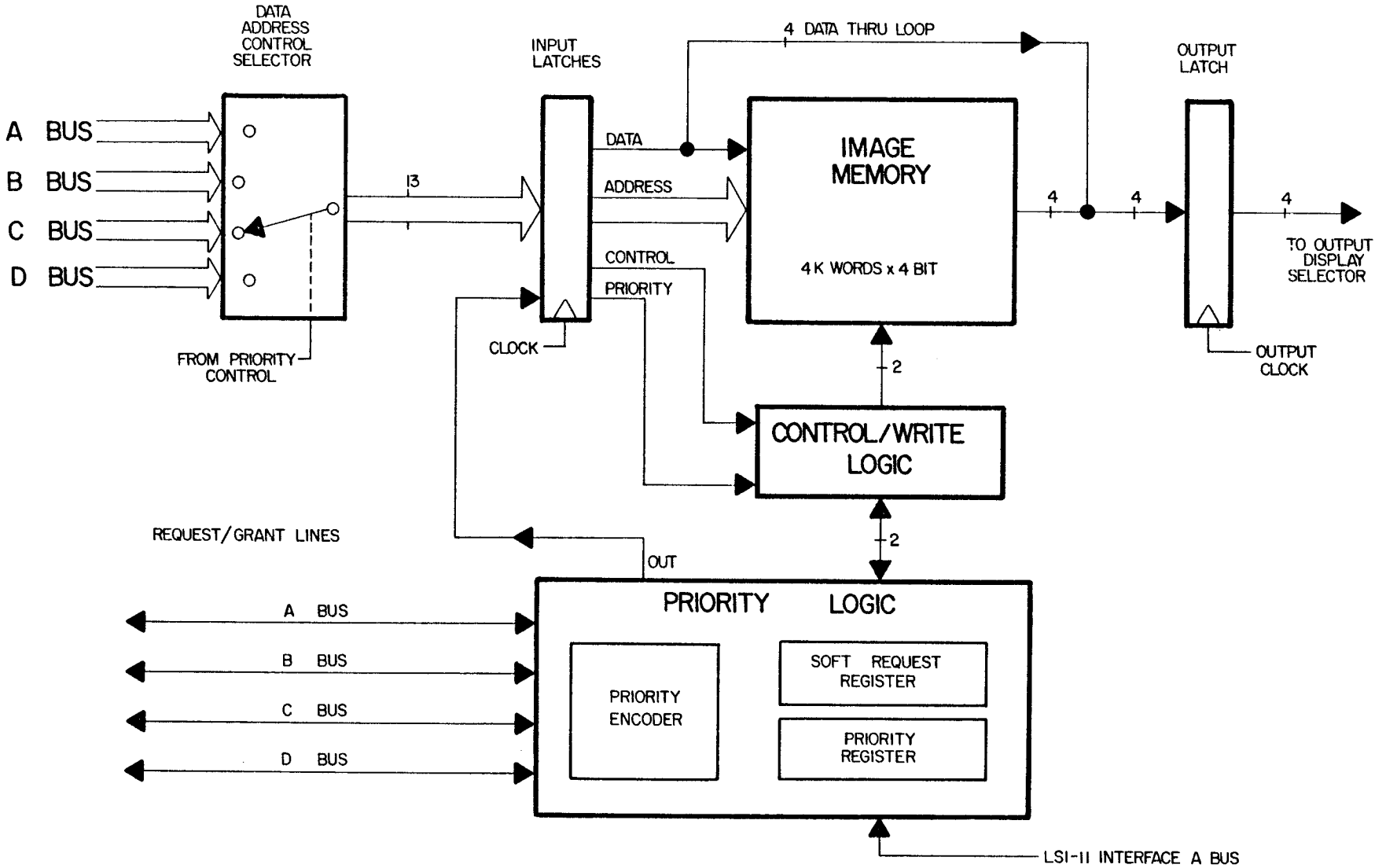


IMAGE BUFFER

(1 OF 8)



Jeff Schier/Don McArthur Digital Image Processor
5/11/92 (F) Jeff Schier

The Schier/McArthur Digital Image Processor was constructed in 1976-1977 at Steina and Woody Vasulka's loft in Buffalo, N.Y. It began as a mathematic exploration by Don McArthur of the digital raster, and was built from digital modules locked to video time by the LSI-11 sixteen bit micro-computer. It was built in stages starting with the sync generator and computer interface, later adding a digital Selector, Arithmetic-Logic Unit, lookup/pattern RAM and a rectangular Window generator. The video outputs came from three 4 bit digital to analog converters, and was converted to color composite video by an external NTSC encoder. The video tape recorder was on a continuous standby, allowing documentation of the design process by Steina Vasulka through "pressing the record button".

The modules were "wire-wrapped" and connected to the computer control and timing bus at the rear of the modules. The digital video paths were patched together with multi-conductor ribbon cables, plugged into the front of each module. External audio could be patched in or out from the front panel, converting the video timing signals to sound. Emphasis was placed on internal square waveforms to form the first pictures, made from the horizontal and vertical bar patterns that subdivide the raster. A borrowed time base corrector was "hot-wired" to pull out 6 bits of live digital video from its A to D converter and color-mapped through the lookup/pattern RAM. A random "power-up" pattern was saved from the RAM and formed a favorite color test pallette for adding colors to the image. The real time remapping of intensity to color formed a color precision (64 levels) unseen in analog colorizers. Dual four bit A to D converters were later constructed to digitally combine two image sources. Operations were performed at 4 bit resolution per red, green and blue channel, but were funneled down to 6 bits when running through the lookup/pattern RAM.

The digital combination of binary images formed unique geometric color patterns. These were unexpected and did not correspond to other analog processes. This became evident when the Arithmetic/Logic Units (ALU's) were installed. The ALU's performed arithmetic functions (addition/subtraction) and logical functions (And, Or, Exor Negation) and wacky mixed arithmetic and logical operations that were "thrown in" by the semiconductor vendor, such as (A OR B plus 1), . The bitwise combination of image combined with overflow-wraparound conditions generated unusual patterns of color and box-like textures, without equivalence in analog video. The binary operations made sense, but the images were a digital surprise. "Official" test images were needed to test out the ALU process. This consisted of a white styrofoam sphere or cone and Woody's hand waved in front of the camera. These test images contain 16 discernible levels of grey, useful to disclose the arithmetic/logical binary

combinations and overflow conditions. The explorations of real time digital video at the Vasulkas predated later image processing and digital video effects units. The exploration of binary operations between images has largely been ignored in image processing and computer graphics, in it's quest for photo-realistic imagery.

Time locked software marching to the video frame rate formed the real time control structure needed to operate the digital image processor. Various test and control table programs were written in Fortran and PDP-11 Assembly language to operate the processing modules. Walter Wright programmed "BARBAR" an assembly language control program with independent timing control stacks. BarBar's timing stacks control processing module functions, time delays, and the looping of the control sequence. The inclusion of random functions exercise the hardware, contributing to long sequences of digital permutations.

Hardware: Consists of a rack of digital processing modules, a gen-locked sync generator, a vertical interval control bus, and a microcomputer to orchestrate the field by field control. The digital video paths for the processing modules are "patched" through their front panels.
Signal Path: Input is received through camera sources, video tape sources, or the internal pattern source (H and V timed bar patterns). For camera/vtr sources, these route through the A/D converters first, are front panel patched to the processing modules, convert back to the D/A converters to R,G,B video and then go to an RGB to NTSC encoder for composite color output for recording and viewing.
1) Micro-computer - A 16 bit DEC LSI-11 microprocessor coordinates control words for the processing modules and handles user interface functions
2) A Vertical Interval Control Buffer and Transfer Bus - Control information is loaded into this control buffer by the microprocessor during the current active field. The data is shipped down to processing modules during the next vertical blanking interval.
3) Processing Modules A) Analog to Digital Converters (A/D) - two 4 bit converters.
B) Selectors - 3 groups of selectors - chooses between 8 horizontal, and 8 vertical frame locked patterns, and an External digital source. The selectors allow bit-wise selection of horizontal, vertical timing components and external video inputs.
C) Arithmetic Logic Units (ALU's) - Combines two digital input streams into a single output through combinations of arithmetic and Boolean logic functions (Output = function (A_in, B_in). The Boolean functions of 'AND', 'OR', 'EXOR', 'EXNOR', Ones Complement are present. The arithmetic 'A PLUS B PLUS CARRY', 'A MINUS B PLUS CARRY', 2's Complement are also available. Certain combination arithmetic with logical operations are possible, with a 'Constant' available on the 'B' input, useful for bit masking.

D) Lookup - an R,G,B lookup table with common digital 'Address input' is present, to perform intensity/pseudo color transformations. The memory could be loaded then scanned out as a small raster.

E) Window generator - three Window generators, form an adjustable frame for gating/routing the digital sources. The frames are independently programmable on a pixel/line basis. Wipe patterns and title boundaries are formed by these.

F) Digital to Analog Converters - one apiece for red, green and blue components at 4 bits per gun.

4) A Gen-Lockable Sync Generator - forms sync timing, and is subdivides the active screen into 512 H by 486 V coordinates. Both video sync and H and V timing information is available on the control bus, for pickoff by modules. A Phase Locked Loop locks the clock timing to an external sync source.

5) RGB to NTSC Color Encoder - the funnel for output, converts the RGB signals from the D/A converters to an NTSC color composite video signal for display and recording onto video tape.

BUFFER BUFFOONERY

AND JUST LOOK AT THOSE FEATURES:

EXPANDING AND SHRINKING
EDGE EXTRACTION
GROWTH OF THE EDGES
IMAGE DECAY
    RANDOM DECAY
    GREY SCALE DECAY
    SPATIAL DECAY
IMAGE REGENERATION - BUILDING UP FROM FRACTURED PIECES
PICTURE PULVERIZATION
COLOR SHIFTING
COLOR EXCHANGE
COLOR MISREGISTRATION - MISPRINTING OF THE RED GREEN AND BLUE COLOR COMPONENTS
DEGRADATION
DESINTIGRATION
COMPOST HEAP MODE
CHARACTER / TEXT GENERATOR
TEXTURAL NEBULIZER
DYNAMIC INTERACTION BETWEEN BUFFERS
MOVEMENT PHENOMENON
DISLOCATION
    TIME
    INFORMATION
    POSITION
FIELD MANIPULATION
MULTIPLE IMAGE INTERPENETRATION
DECAY MODE
MOIRE GUN
COLOR BANDING
COLOR BENDING
IMAGE WARPING
NON OPTICAL IMAGE AND SOUND EXTRACTION (NOISE)
AUDIO
COLOR CORRUPTION
RETIMING OF VIDEO
FREEZE FRAMING
KEYING
MULTIUDIMENSIONAL WIPES
FEEDBACK BETWEEN BUFFERS
HORIZONTAL AND VERTICAL DELAY LINES
PANCAKE AND WAFFLE MODE
EGG EXTRACTION
    SCRAMBLING
    POACHING
    CODDLING
    FRYING
    ONCE OVER LIGHTLY
    HARD BOILED
    OMELET
    WESTERN
FOOD PROCESSING
    JUICING
    DICING
    SLICING
    CRUSHING
    SLITTING
    PITTING
GREY SCALE COMPACTOR

DISCNAME: JEFFY
FILENAME: EMULO.TXT
UPDATED: 2-JUL-78

IMAGE EMULSIFIER OVERVIEW

BY JEFFY SCHIER

THIS IS A SHORT OVERVIEW ON THE CHARACTER OF THE ELECTRONIC 'IMAGE EMULSIFIER.' THE EMULSIFIER WILL CAPTURE IMAGES AND ENCASE THEM WITHIN FINE MESHES OF STORED LIGHT (IMAGE BUFFERS). THESE MESHES ARE TREATED AS ELASTIC MEMBRANES OF COLOR AND TEXTURE, UNDER THE SCRUTINY OF A DIGITAL DEMON (THE VIDEO PROCESSOR).

ONCE AN IMAGE IS STORED, IT IS CODED MATTER, ELECTRICAL FUEL FOR FURTHER ORGANIC AND MECHANICAL ABSTRACTION. TO FULFILL THIS, THE DEMON IS INSTRUCTED (MICROPROGRAMMED), TO CREATE VISUAL PHENOMENA INCLUDING:

MELTING PICTURES INTO FROSTY PUDDLES OF DRIPPING COLOR
COAGULATING AND GRAFTING GREY-SCALES BETWEEN IMAGE PLANES
GROW IRIDESCENT CRYSTALINE SPIRES, FROM EXTRACTED EDGES
KNEAD, WARP, PULVERIZE AND SHATTER IMAGE BY SPATIAL AND SPECTRAL DECAY
GIVE BIRTH ON SCREEN, TO NON OPTICAL IMAGES FOR SOUND EXTRACTION (NOISE)

THIS PROJECT INVOLVES MERGING THE DIVERSE METHODS OF VIDEO, DIGITAL ELECTRONICS, AND COMPUTER TECHNOLOGIES; TO EVOLVE A NEW GENERATION OF IMAGING TOOLS.

BUFFER BUFFOONERY

AND JUST LOOK AT THOSE FEATURES:

EXPANDING AND SHRINKING
EDGE EXTRACTION
GROWTH OF THE EDGES
IMAGE DECAY
    RANDOM DECAY
    GREY SCALE DECAY
    SPATIAL DECAY
IMAGE REGENERATION - BUILDING UP FROM FRACTURED PIECES
PICTURE PULVERIZATION
COLOR SHIFTING
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COLOR MISREGISTRATION - MISPRINTING OF THE RED GREEN AND BLUE COLOR COMPONENTS
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DYNAMIC INTERACTION BETWEEN BUFFERS
MOVEMENT PHENOMENON
DISLOCATION
    TIME
    INFORMATION
    POSITION
FIELD MANIPULATION
MULTIPLE IMAGE INTERPENETRATION
DECAY MODE
MOIRE GUN
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FREEZE FRAMING
KEYING
MULTIUDIMENSIONAL WIPES
FEEDBACK BETWEEN BUFFERS
HORIZONTAL AND VERTICAL DELAY LINES

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0.0 SYNOPSIS

This guide describes the functional and programming aspects of the Schier/MacArthur Imaging Bus (henceforth the S&M bus). This device is an interface from digital computer (LSI-11) to video. The system is physically modular in nature, and therefore facilitates a wide variety of operational modes.

The functions of these modules and the effects they manifest are similar to that of an all-analog processing environment; where some modules act as generators of video, like analog oscillators, while others act as filters or processors of an input video signal. The difference lies in that the S&M modules deal exclusively with video as a digitized stream of bits, which can be generated internally provided from an external source such as a digitized TV camera image, or a mixture of these. In either case the bit streams are converted to analog voltages to produce a conventional video signal.

Although the modular nature of the S&M bus doesn't offer much in the way of friendliness to the user unaccustomed to the ways of digital, the modularity provides a most fertile structure for the exploration of a vast variety of control structures. Approximately 100 device registers facilitate computer program control over real-time processing and synthesis of video. Any or all of these control registers may be modified as often as field rate (1/60th of a second).

0.1 ENVIRONMENT HISTORY

The S&M bus was designed for the Vasulkas by Don Mac Arthur in 1976. Since then, 5 modules have been designed and implemented on the bus, most by Jeffy Scheir. The host processor is a Digital Equipment Corporation LSI-11 with 48 kilobytes of memory and dual floppy-disk drive. Control of the S&M bus by the processor is implemented via approximately 100 device registers which are mapped into LSI-11 address space in the range of 171000 to 171776 octal.

0.2 PHYSICAL LAYOUT

The S&M bus is a card rack containing 8 modules; the sync generator, 2 for the processor interface, and 5 programmable modules. The sync generator provides timing for the bus and is gen-lockable to an external video source. The processor interface modulesare connected by ribbon cable to an interface card residing in the LSI-11 backplane.

The inputs and/or outputs of each module are present on 16 pin DIP connectors on the front panel. Pinout conventions are such that any single output can safely drive any reasonable number of inputs. Two outputs may not be tied together. The DIP connectors are conected to one another by ribbon cable patch cords. The particular pinins and pinouts will be discussed with each module.

1.0 PROCESSOR INTERFACE

The S&M bus shares 256 words of buffer memory with the LSI-11. These locations behave to the LSI-11 just like read-write memory locations. At regular interval, usually video field rate, the contents of this buffer memory is transferred to device registers on the S&M bus. This event can be enabled/disabled in software via the S&M bus status and control register.

1.1 BUS CONTROL REGISTER - 171776

Bit 0 of this register is currently the only one implemented. On LSI-11 bus reset and power-up, this bit is cleared to 0. Any modifications made to the buffer memory by software will have no effect on the device registers since the transfer is not enabled. When this bit is set by software, the buffer memory to device register transfer is enabled. During the actual transfer, buffer memory cannot be accesed by the LSI-11, and a bus timeout trap will occur if an attempt is made to do so. Setting this bit also has other implications; at the end of buffer transfer, the S&M interface issues an interrupt to the LSI-11, causing the processor to fetch a new PC and PS from address 170 octal. Software must deal with this; an example of how to set up and service the S&M device is depicted thusly

```
START: MOV #SMSERV,@#170      ;PUT ADDRESS OF SERVICE ROUTINE
       MOV #0,@#172           ;AND PROC. STATUS WORD
                              ;IN VECTOR LOCATION
       BIS #1,@#171776        ;ENABLE TRANSFER-INTERRUPT
LOOP:  BR LOOP                ;WAIT FOR INTERRUPT OR GO ON
                              ;ABOUT BUSINESS.
                              ;
; FOLLOWING ROUTINE IS CALLED BY S&M HARDWARE INTERRUPT
; AT THE END OF A BUFFER TRANSFER

SMSERV: BIC  #1,@#171776      ;DISABLE INTERRUPT-TRANSFER
       JSR  PC,BUFSERV        ;CALL SOME ROUTINE THAT UPDATES-ACCESSES
                              ;S&M BUFFER MEMORY
       BIS #1,@#171776        ;REENABLE INTERRUPT
       RTI                    ;AND RETURN
```

2.0 X Y COUNTER MODULE

This module is based around two independant 8 bit up counters. The X counter uses a pixel rate clock as input. The y counter uses a horizontal line rate clock. Both these clocks may be divided by a value from 1 to 16 before being input to the counters.

2.1 ZOOM REGISTER - 171052

The lower nybble of each byte of the zoom register control the divisor by which the respective clock is divided; 0 = divide by 1, 15 = divide by 16. It is termed the zoom register because of the visual effect it produces.

2.2 SHIFT REGISTER - 171050

At the start of an active field, both the X and Y counters are reset to the values contained in this register. The counters will then proceed to count up from that value, wrapping around to 0 when reaching 255.

2.3 X Y COUNTER PIN ASSIGNMENTS

PIN	SIGNAL	PIN	SIGNAL
1	X0	9	Y0
2	X1	10	Y1
3	X2	11	Y2
4	X3	12	Y3
5	X4	13	Y5
6	X5	14	Y5
7	X6	15	Y6
8	X7	16	Y7

3.0 DATA SELECTOR MODULE

This module consists of twelve 16 to 1 data selectors. It permits the channeling of any one of 16 inputs to any of twelve outputs. Also, any of these outputs may be selectively inverted. The data selector is housed in the same module and above the X Y counter module. A conceptual block diagram of the data selector follows

3.1 SELECTION REGISTERS - 171040 RED
171042 GREEN
171046 BLUE

There is one selection register for every 4 bits of output. These 3 groups of 4 bits are arbitrarily referred to as red, green, and blue. This convention is purely a mental one. Any one of the 16 inputs may be directed to a particular output by placing the input channel number in the appropriate output bit field of a selection register. For example; placing the pattern 1010101010101010 (125252 octal) in the red selection register would channel input number 10 to all 4 bits of the red output group.

3.2 INVERSION REGISTER - 171046

The twelve outputs from the data selector section can each be complemented by placing a 1 in the appropriate bit of the inversion register. A 0 will pass the respective channel unchanged.

3.3 DATA SELECTOR PIN ASSIGNMENTS

INPUT CONNECTOR ASSIGNMENTS

PIN	SIGNAL	PIN	SIGNAL
1	CHAN0 INPUT	9	CHAN8 INPUT
2	CHAN1 "	10	CHAN9 "
3	CHAN2 "	11	CHAN10 "
4	CHAN3 "	12	CHAN11 "
5	CHAN4 "	13	CHAN12 "
6	CHAN5 "	14	CHAN13 "
7	CHAN6 "	15	CHAN14 "
8	CHAN7 "	15	CHAN15 "

OUTPUT CONNECTOR ASSIGNMENTS

PIN	SIGNAL	PIN	SIGNAL
1	RED0 OUTPUT	9	BLUE0 OUTPUT
2	RED1 "	10	BLUE1 "
3	RED2 "	11	BLUE2 "
4	RED3 "	12	BLUE3 "
5	GREEN0 OUTPUT		
6	GREEN1 "		
7	GREEN2 "		
8	GREEN3 "		

4.0 WINDOW MODULE

The window module generates 3 so-called windows: a set of 4 edges, two vertical (X), two horizontal (Y) (with respect to the frame). The position of each edge and how the inside and outside are defined are under software control.

There are 3 duplicate window generating channels, Red, Green, and Blue. Each channel has 4 position control registers designated X1 Y1 X2 Y2. Each X and Y pair generate a pulse whose starting and ending times correspond to the value in the respective registers. Thus

WINDOW ALU: RED — 17030
GREEN — 52
BLUE — 34

4.1 EDGE POSITION REGISTERS

The lower 9 bits of each edge position register control the postion of each edge of the window in the field. The X1 and Y1 registers control the leading edge, the X2 and Y2 registers control the trailing edge. The way these values map into the field is depicted as follows

WINDOW EDGES :

RED X_1 - 171000

RED Y_1 2

RED X_2 4

RED Y_2 6

GREEN 171010 X_1

2 Y_1

4 X_2

6 Y_2

BLUE 171020

2

4

6

4.2 WINDOW FUNCTION ALU

The x and y pulses of each of the three channels are input as operands to three ALUs. These sections control the way the inside and outside are derived from the X Y pulse pair. The output of the ALUs are used as a key which switches between two inputs, or one input and black.

Window ALU WALUR-R - 171 030

WALUG-G - 2

WALUB-B - 4

4.3 WINDOW MODULE PIN ASSIGNMENTS

A AND B INPUT CONNECTOR PIN ASSIGNMENTS

PIN	SIGNAL	PIN	SIGNAL
1	RED0 INPUT	9	BLUE0 INPUT
2	RED1 "	10	BLUE1 "
3	RED2 "	11	BLUE2 "
4	RED3 "	12	BLUE3 "
5	GREEN0 INPUT		
6	GREEN1 "		
7	GREEN2 "		
8	GREEN3 "		

OUTPUT CONNECTOR PIN ASSIGNMENTS

PIN	SIGNAL	PIN	SIGNAL
1	RED0 OUTPUT	9	BLUE0 OUTPUT
2	RED1 "	10	BLUE1 "
3	RED2 "	11	BLUE2 "
4	RED3 "	12	BLUE3 "
5	GREEN0 OUTPUT		
6	GREEN1 "		
7	GREEN2 "		
8	GREEN3 "		

5.0 ALU MODULE

This module is based around three 4-bit wide ALUs. They are arranged as 3 independant channels and are designated Red, Green, and Blue. The Arithmetic Logic Unit performs performs mathematical operations on 2 operands: A and B. Software can select any one of 64 operations for each ALU, as well as selecting one of two sources as the A operand, and one of four sources as the B operand.

5.1 ALU CONTROL REGISTERS - 171000 RED
171004 GREEN
171010 BLUE

Bit 10 selects the source of the A operand. Bits 8 and 9 select the source of the B operand, while bits 0 through 5 control the function performed on the A and B operands by the ALU.

5.2 ALU NUMERIC REGISTERS - 171102 RED
171106 GREEN
171112 BLUE

The A operand comes form 1 of 2 sources; the color group input comes from the A input connector. Each color is associated with the ALU of that color. The other possible source for the A operand is from the Numeric Data Register . There is one register for each of the 3 ALUs. This way software provides the value for the A operand to the ALU.

The B operand can come from one of 4 sources. 3 are any one color group from the A input connector. The fourth possible input is from the external connector.

5.3 ALU PIN ASSIGNMENTS

A OPERAND INPUT CONNECTOR

PIN	SIGNAL	PIN	SIGNAL
1	RED0 INPUT	9	BLUE0 INPUT
2	RED1 "	10	BLUE1 "
3	RED2 "	11	BLUE2 "
4	RED3 "	12	BLUE3 "
5	GREEN0 INPUT		
6	GREEN1 "		
7	GREEN2 "		
8	GREEN3 "		

EXTERNAL OPERAND INPUT CONNECTOR

PIN	SIGNAL	PIN	SIGNAL
1	REXT0 TO RED ALU	9	BEXT0 TO BLUE ALU
2	REXT1 "	10	BEXT1 "
3	REXT2 "	11	BEXT2 "
4	REXT3 "	12	BEXT3 "
5	GEXT0 TO GREEN ALU		
6	GEXT1 "		
7	GEXT2 "		
8	GEXT3 "		

6.0 MEMORY MODULE

This module is based around a 64 by 16 bit array of high-speed RAM (read-write memory). Software can control the source of data and address for the RAM, including loading the data from memory data registers which are accessable to the LSI-11 . In addition, a 'write then display' mode can be selected whereby the contents of the high-speed RAM are updated automatically during vertical interval, and then switched to display during the active field.

6.1 MEMORY CONTROL REGISTER - 171170

One of 2 sources may be selected as the data source for the high-speed RAM. If bit 3 in the Memory Control Register is cleared to 0, the RAM will receive data from the S&M/LSI-11 buffer memory, that is the Memory Data Registers. These registers appear to the LSI-11 as write only; the contents of the RAM cannot be read back by software. If bit 3 of the Memory Control Register is set to 1, the RAM will receive data from the external data connector.

If bits 1 and 2 of the Memory Control Register are set to 0 (00 binary), the address information comes from the S&M/LSI-11 buffer memory, which is active during vertical interval. Therefore, if this source is selected, (and the write-then-display bit is 0), the output of the RAM during the active field will be the contents of the highest address of RAM. This is because when the S&M processor interface performs transfer during the vertical interval, it sweeps up through all the addresses from lowest to highest. And the last address presented to the high-speed RAM is the highest one; that which corresponds to the memory data register addressed at 171376.

When the address source select bits are set to 2 (10 binary), the address source is from extenal connector 0, and when the address source select bits are set to 3 (11 binary), from external connector 1.

6.2 MEMORY SHIFT REGISTER - 171172

If the address source select bits are set to 1 (01 binary), the address source will be an X Y counter, similar to the one in the X Y counter module. When its source is selected, the memory will be scanned out sequentially during the active field as an array of 8 horizontal by 8 vertical elements, each 16 bits deep. The starting address of the memory X Y counter may be set by software via the Memory Shift Register. The memory will be read out starting at the address specified in this register, wrapping around to address 0 when reaching address 63.

6.3 WRITE THEN DISPLAY

Bit 4 of the memory control register, when set to 1, selects the write-then-display feature. Conceptually, this bit ORs vertical blanking with the lower bit of the address source select (bit 1). This then causes the memory to switch its address from one source during vertical blanking (write), to another source during the active field (then display). So when this feature is enabled, the memory will switch between either S&M bus and X Y, or between external 1 and external 2. If the former pair are selected (address bits = 00, W.D. Bit = 1) then the RAM will be updated from the Memory Data Registers during vertical blanking, and then displayed in the 3 x 8 format during the active field.

6.4 MEMORY MODULE PIN ASSIGNMENTS

EXTERNAL 0 & 1 CONNECTORS

PIN	SIGNAL
1	ADDR0 LSB
2	ADDR1
3	ADDR2
4	ADDR3
5	ADDR4
6	ADDR5 MSB

EXTERNAL DATA INPUT CONNECTOR

PIN	SIGNAL	PIN	SIGNAL
1	DIN0 LSB	9	DIN8
2	DIN1	10	DIN9
3	DIN2	11	DIN10
4	DIN3	12	DIN11
5	DIN4	13	DIN12
6	DIN5	14	DIN13
7	DIN6	15	DIN14
8	DIN7	16	DIN15 MSB

DATA OUTPUT CONNECTOR

PIN	SIGNAL	PIN	SIGNAL
1	DOUT0 LSB	9	DOUT8
2	DOUT1	10	DOUT9
3	DOUT2	11	DOUT10
4	DOUT3	12	DOUT11
5	DOUT4	13	DOUT12
6	DOUT5	14	DOUT13
7	DOUT6	15	DOUT14
8	DOUT7	16	DOUT15 MSB

7.0 EXPORT/IMPORT MODULE

This module facilitates transfer of parallel data to and from external devices and/or other modules. The module supports 4 16-bit output ports and 2 16-bit input ports.

7.1 EXPORT IMPORT DATA REGISTERS

171070 EXPORT0
171072 EXPORT1
171074 EXPORT2
171076 EXPORT3

171600 IMPORT0
171602 IMPORT1

Each port is associated with a data register. As with all the modules, the inputs and outputs are Low Power Schottky TTL, and all rules for this type of signal apply. The outputs will drive any reasonable number of L S TTL inputs; but no two outputs should ~~not~~ be tied together.

7.2 EXPORT/IMPORT PIN ASSIGNMENTS

EXPORT CONNECTORS 0 - 3

PIN	SIGNAL	PIN	SIGNAL
1	OUT0 LSB	9	OUT8
2	OUT1	10	OUT9
3	OUT2	11	OUT10
4	OUT3	12	OUT11
5	OUT4	13	OUT12
6	OUT5	14	OUT13
7	OUT6	15	OUT14
8	OUT7	16	OUT15 MSB

IMPORT CONNECTORS

PIN	SIGNAL	PIN	SIGNAL
1	IN0 LSB	9	IN8
2	IN1	10	IN9
3	IN2	11	IN10
4	IN3	12	IN11
5	IN4	13	IN12
6	IN5	14	IN13
7	IN6	15	IN14
8	IN7	16	IN15 MSB

8.0 S&M BUS REGISTERS AND MNEMONICS

8.1 WINDOW MODULE -

171000	REDX1	WINDOW EDGE POSITIONING
171002	REDY1	
171004	REDX2	
171006	REDY2	
171010	GRENX1	
171012	GRENY1	
171014	GRENX2	
171016	GRENY2	
171020	BLUEX1	
171022	BLUEY1	
171024	BLUEX2	
171026	BLUEY2	
171030	WALUR	WINDOW FUNCTION ALU'S
171032	WALUG	
171034	WALUB	

8.2 DATA SELECTOR MODULE -

171040	REDSEL	DATA SELECTOR SOURCE SELECT
171042	GRNSEL	
171044	BLUSEL	
171046	SELINV	INVERSION REGISTER

8.3 X Y COUNTER -

171050	SHIFT	X Y COUNTER INITIAL VALUE
171052	ZOOM	" COUNT RATE DIVIDE

8.4 ALU MODULE -

171100	ALURED	ALU FUNCTION-INPUT SELECT
171102	NUMRED	ALU B-INPUT OPERAND
171104	ALUGRN	
171106	NUMGRN	
171110	ALUBLU	
171102	NUMBLU	

8.5 HIGH SPEED MEMORY MODULE -

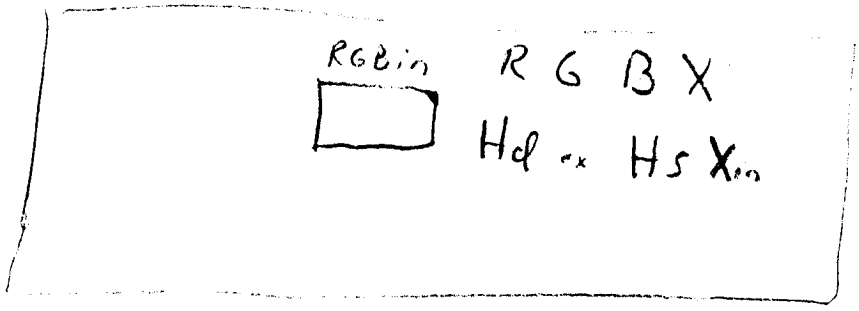
171170	MEMSTA	MEMORY STATUS
171172	MEMSHF	MEMORY DISPLAY SHIFT
171200	MEMORY	MEMORY DATA REGISTERS
171376	MEMORY	" " "

8.6 EXPORT/IMPORT MODULE -

171070	EXPRT0	PARALLEL OUTPUT PORT
171072	EXPRT1	
171074	EXPRT2	
171076	EXPRT3	
171600	IMPRT0	PARALLEL INPUT PORT
171602	IMPRT1	
171606	INDEX	FIELD ODD-EVEN INDEX

8.7 S&M BUS CONTROL -

171776	STATUS	S&M BUS STATUS AND CONTROL



The RGB outputs (Mini BNC) go to the Processor. The Hd is the Horizontal drive from the Color proc.

Hs is the Horizontal Sample, should be the same freq as Hs - (Not used normally)

Xin is An input for the Dot clock - Not Norm. Used

Xout is the Xclk - dot clock that goes to the McArtur.

RGB in goes to the McArtur.

Boots on power up - BS @ 173000

Left drive is dy0 or dk0

Right is dy1 or dk1

emulates an RX02

RT-11 V5.00 ~~has a help function.~~

Just type help ↵ for instructions

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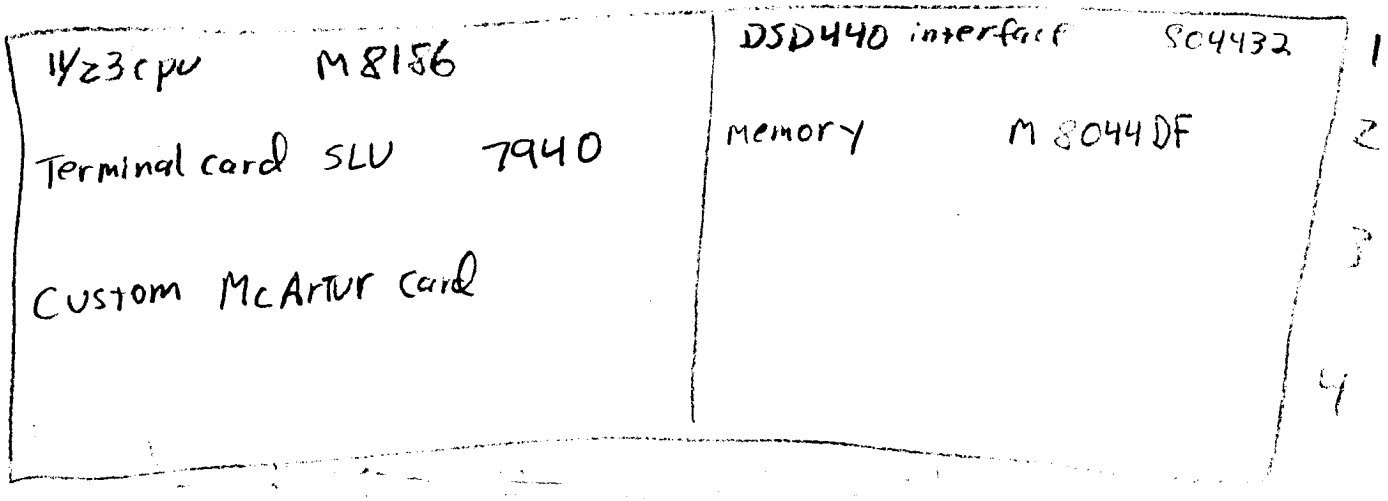
from ODT reboot with 173006

Hardware config



Terminal cable has

Disk cable has TOP written on it and its keyed.

McArtur cable has TOP on it also

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Education : **BSEE 1978, State University of N.Y. Buffalo**

Work Experience :

1987-1989 : Pinnacle Systems

Project Manager - developed *PriZm* digital video effects system (DVE). Defined architecture and coordinated implementation from prototype through production. The DVE performs real-time rotation, perspective transformations, and curved/warping of the image; with the aid of a color menu interface. The DVE was integrated within a Video Workstation line merging still-storage, digital video effects, and paint/3D animation. System processing was based upon an 80286 user interface, with an 80386/80387 coordinate processor. The (4:2:2:4) pixel pipeline includes adjustable FIR filters, random access transformation memory, and table driven address generation. Designed and implemented the transformation memory. Logic design and PCB layout centered around 80386 computers using PCAD, ORCAD, CUPL, ABEL, Microsoft C and Assembler under MS-DOS. ASIC development using Xilinx and Actel chips. Application is in industrial/broadcast video.

1990- Present: Chips and Technologies, Inc. Staff Design Engineer

1985-1987 : Aurora Systems

Senior R+D Engineer - Development of multi-port image memory, with bit-slice controller for a 32 bit, full color "AU280 Paint System". The frame buffers operate at video rates, for real-time image processing on multiple data streams. The image subsystem lives on a VME bus, driven by a SUN 3/68020 computer. Hardware development was centered around a Valid Scald workstation, with PAL/PROM logic programming/simulation using ABEL.
Application is in broadcast television and commercial computer graphics.

1983-1985 : Cubicomp Corp.

Senior Research Engineer - Hardware/software development of 3-D Solid Modeling system running on IBM PC/PC-AT. New product definition, hardware/diagnostics, Gen-Lock/Video Compatibility, Color Encoder/Keyer, Matrix QCR Support, Inkjet Printer software drivers.

1980-1983 Grinnell Systems

Senior Research Engineer : Lead design of GMR2800 Computer Graphics Image Processing system. System is bit-slice (AMD2900) based, with memory feedback pipeline for image processing. Microcode compiler/assembler developed in-house. Implementation of sync timing, gen-lock, Flash A/D Converter, D/A Converter, EIA Sync Drivers, Multi-mode computer interfaces (DEC Unibus and Q-bus).

1979-1980 Nicolet-Cad Corporation

Project Leader for Color graphics CAD Workstation applied to PC board design. Design of overlay card, sync/timing generation, Image memory, Bit-slice graphics processor enhancements.

1976-1979 Vasulka Corporation

Design Engineer. Software/Hardware interface of unique Video processing machines to DEC LSI-11 microcomputer : George Brown Multi-level Keyer, Seigel Colorizer, Rutt/Etra Scan processor. Co-Design of McArthur/Schier real-time Image processor. Full design and implementation of Image Articulator : a bit-slice based frame buffer with real time image manipulation abilities. Production in 3/4" Umatic, 1/2" EIAJ tape formats.

Programming Languages : **C, Fortran, Assembler, Microcode**
Operating Systems : **UNIX, MS-DOS, DEC RT11/RSX11M**

Video Workshops : **S.U.N.Y. Buffalo, Media Study Buffalo**
Papers : **"Merging of 2D and 3D effects", SMPTE 1988 conference N.Y.**
"Video Architectures - Approaching Real Time", Wescon/Northcon 1985
IEEE C.G+A, Feb. 1986 - "Cherries in Needlepoint Texture"
Member of SMPTE and ACM/SIGGRAPH

References furnished upon request.