NEA Report

I. Introduction

As science advances, with the resulting advances in technology, we have new tools and new capabilities which influence our world in many ways. This new technology not only influences the traditional art forms but also produces new forms of art. The development of high speed electronic components and circuits, the cathode ray tube, the video camera, and inexpensive video tape recorders enabled the development of video art. The development of small but powerful computers now allows systems to be developed which can give the video artist a new dimension of control over the video image. With a computer-based video synthesizer (CBVS), one can generate a sequence of images while controlling each individual image with detail and precision that is many orders of magnitude greater than is possible with manual control.

The ability to control the dynamics of the image is useful to the artist only if the system is capable of generating the image in real time. With this requirement in mind, the natural choice of devices for converting electrical signals to visual images is the conventional video system. This choice also gives the capability of recording the video compositions with a conventional video tape recorder and of broadcasting to a large audience through existing network systems.

There are basically two modes of operation of the system: interactive compositional mode and automatic production mode. In the compositional mode, the artist can enter programs and parameters through the keyboard, observe the resulting sequence of images, and then modify parameters through either the keyboard or a real time input and thus build up a data set for a complete piece. At each stage of the composition process the data set, representing all the aesthetic decisions made by the artist, is stored in the computer. When the composition is finished the system will operate in the automatic production mode generating the final video signal in real time with no intervention by the artist. The artist may also choose to use a combination of these two modes in an interactive performance or allow an audience to interact with the system operating automatically. The system is structured so that all of these variations can be accomodated by appropriate programming.

The system may be operated as a generating synthesizer which produces a video signal entirely from internal signals or as a processing synthesizer which utilizes signals of external origin such as a video camera. Either of these two types of operations is carried out by a configuration of element modules, each of which performs a class of functions, with the specific function during one frame being determined by the control parameters received from the computer.

Since the computer functions only to generate the parameters which govern the behavior of the synthesizer modules, a video signal will be generated without operation of the computer. The system will simply repeat the frame until the parameters are changed. Thus the artist may choose to stop the computer in which case he is able to examine a single frame, or he may alter the program so that a given sequence is displayed very slowly or repeated very rapidly.

II. System Structure

The CBVS consists of two parts: the computer section shown in the lower section of figure 1 and the video section shown in the upper section of the figure. Both sections operate simultaneously and independently, communicating through the buffer memory which has a capacity of 1,024 16 bit words. Each of these words is either a picture element, a number which controls some function of the video section and determines some aspect of one field of the video image, or it is a picture feature, a number determined by the video section and may depend on an external signal such as a video camera signal. The buffer memory is connected to the computer bus through a 16 bit parallel interface which is structured in such a way that each word in the buffer memory is addressable and may be read or written in exactly the same way as words in the main computer memory. This memory-mapped I/O system simplifies the software which controls the buffer memory. In order to update an element such as a control D/A, the computer must execute an instruction which stores the new value in the location corresponding to that element.

During the active scan time, the control computer reads features from the buffer memory and generates elements for the following field and stores them in the buffer memory. During the vertical blanking interval, information is transferred through the element bus from the buffer memory to the element modules or from the feature modules to the buffer memory. The designation of a particular area of the buffer memory as an element or feature is under program control. During the transfer between the buffer memory and the element bus, the computer is locked out of the buffer memory. On completion of the transfer, the interface generates a vectored interrupt which requests the computer to generate parameters for the next field.

The computer system consists of: a DEC LSI-11 microprocessor which has a 16 bit word length and an instruction execution time of about 7 microseconds; Teletype Keyboard and printer connected through a serial interface; 20 K of dynamic memory; a dual drive floppy disk system with a capacity of 256,256 bytes per diskette. An additional serial interface is also available for connecting through a modem to other computer systems. The entire system is dedicated to the synthesizer system.

The overall timing is determined by a 9.7552434 MHz clock which is phase locked to the subcarrier (3.579545 MHz). This frequency is chosen to insure a coherent subcarrier and to divide the active portion of the scan line into 512 pixels. The red, green, and blue signals are generated independently, and the chroma encoding is done with analog circuits; thus there is no advantage to following the common practice of making the pixel rate an integer multiple of the subcarrier frequency. With this clock frequency, a full nine bit word is used to define the horizontal position on the active portion of the raster. Figure 2 shows the X and Y wave forms. The X-Y module generates twenty bits of timing information (ten bits for horizontal, including the blanking period, and ten for the line count). This module also generates sync, drive, burst flag, and the transfer request $\overline{TR}$ signal which controls the timing of the buffer memory.

Timing details of the interface and buffer memory are shown in figure 3. The transfer request $\overline{TR}$ goes low at the beginning of vertical blanking initiating an arbitration for access to the buffer memory. If the computer is accessing the buffer memory, the current bus cycle is completed, then $\overline{READY}$ goes high, and the buffer memory controller cycles through memory making the required element and feature transfers. When this is completed, $\overline{READY}$ goes low, control of the memory is returned to the computer, and an interrupt is generated requesting data for the following field. As indicated in the diagram, during the Nth field, the computer is generating data for the N+1th field.

The timings of the signals on the element bus are indicated in figure 4. During the transfer, the memory controller generates: the addresses $A_{\overline{CME}}$ -A_0 ; the clock signals $\overline{\phi_1}$, $\overline{\phi_2}$, and $\overline{\phi_3}$; and the status signals $\overline{CME}$ indicating a transfer from the memory to an element and $\overline{CFM}$ indicating a transfer from a feature module to the memory. The signals $\overline{ETF}$ and $\overline{FTE}$ are generated by the synthesizer modules and initiate a controller Element/Feature mode change. The three phase clock system is used to control modules which have the structure shown in figure 5. Functions which use data from the computer during the vertical blanking interval are disabled when the buffer memory accesses that particular element by a signal generated using $\overline{\phi_1}$. This allows access to the buffer memory during $\overline{\phi_2}$. The third clock, $\overline{\phi_3}$ generates a memory write signal.

Time delays in the digital processing modules could produce errors and shifts of the image to the right. This is prevented by deskewing the output of each with a latch clocked by the master clock (9.755 MHz.). Compensation for the resulting 102.5 nSec. delay in each module is provided by starting the X count at the beginning of the horizontal blanking interval rather than at the end. An additional shift to the right or left is then achieved by adding (mod 512) a constant supplied by the computer. The default value of this constant is 404 + number of elements.

III. Element and Feature Modules

The structure described above supports a variety of element and feature modules which may be chosen and configured according to the tastes of the artist. Our experience indicates that a large amount of work can be produced with a relatively small number of elements in a standard configuration. Whenever possible, a new element added to the system is configured in such a way that if the control word is set equal to zero it has no effect on the system. Thus a minimum amount of reprogramming is required following system expansion.

Two general classes of modules have been developed: digital and hybrid. The hybrid elements are: high-speed D/A converters used for generating the red, green, and blue video signals which are converted to NTSC format in the standard way: low-speed D/A converters used for generating control voltages, field-by-field controllable, used to operate existing voltage controlled analog image processing systems such as keyers, raster manipulaters, etc. Another hybrid element is the analog video switching matrix. Four bits of one control word are used to select one of sixteen inputs for one output.

Digital processing elements include: constant; X + constant; Y + constant; twelve-channel sixteen-line demultiplexer with output complement; and four-channel four-bit by sixty-four word memory.

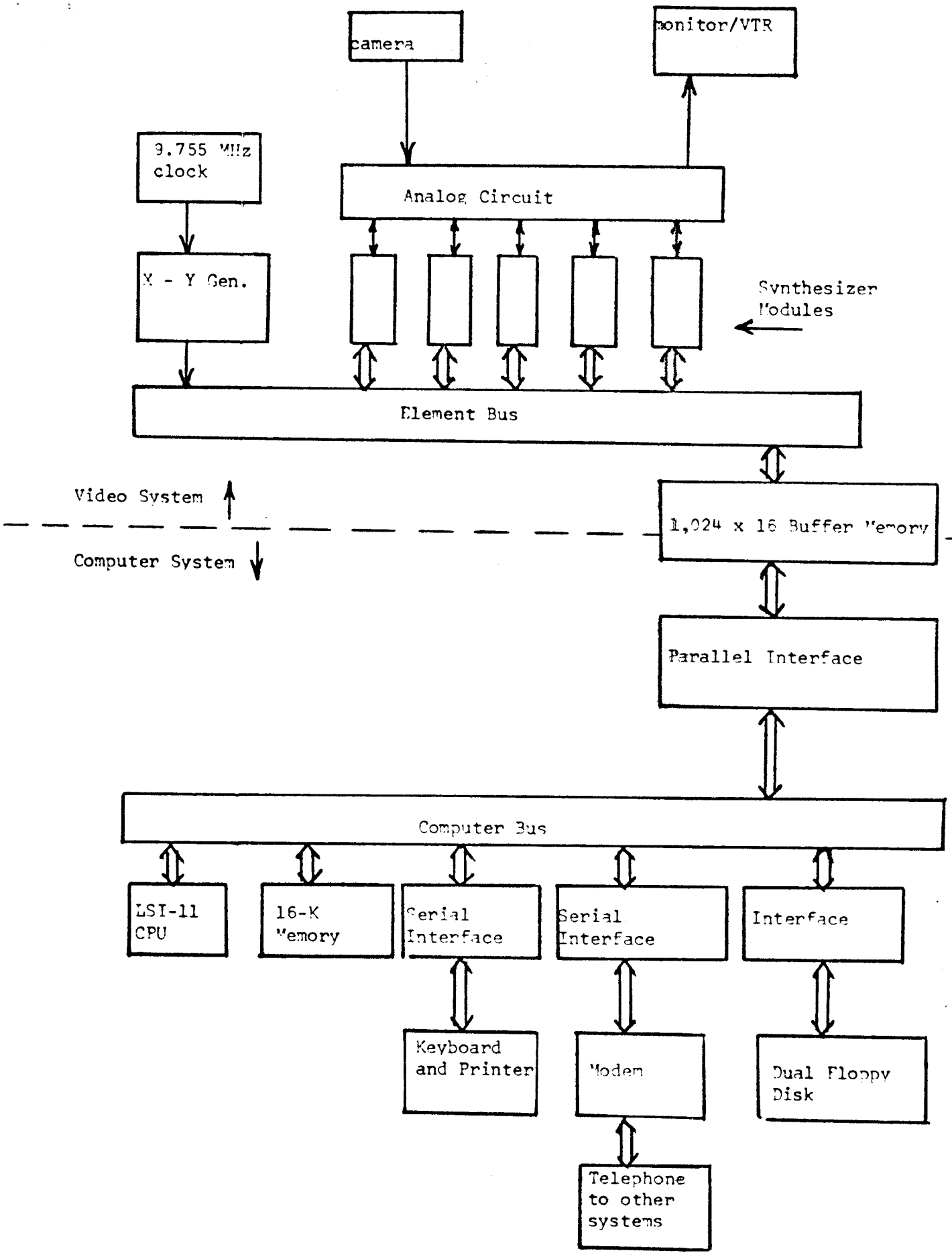

camera
monitor/VTR
9.755 MHz clock
Analog Circuit
X - Y Gen.
Synthesizer Modules
Element Bus
Video System
Computer System
1,024 x 16 Buffer Memory
Parallel Interface
Computer Bus
LSI-11 CPU
16-K Memory
Serial Interface
Serial Interface
Interface
Keyboard and Printer
Modem
Dual Floppy Disk
Telephone to other systems

Figure 1

X and Y Half Cycle Durations and Wave Forms

x_1 102.5 nSec.

x_2 205 nSec.

x_3 410 nSec.

x_4 820 nSec.

x_5 1.64 μSec.

x_6 3.28 μSec.

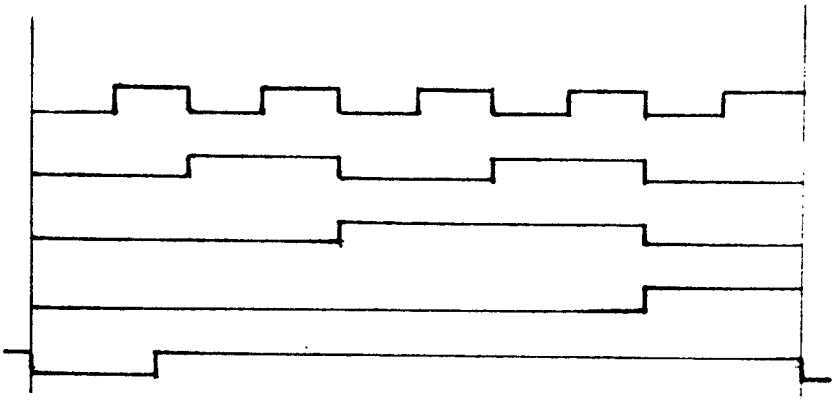
x_7 6.56 μSec.

x_8 13.12 μSec.

x_9 26.24 μSec.

x_{10} 52.48 μSec.

Horizontal Blanking



y_1 16.66 mSec.

Field Index

y_2 63.5 μSec.

y_3 127 μSec.

y_4 254 μSec.

y_5 508 μSec.

y_6 1.01 mSec.

y_7 2.03 mSec.

y_8 4.06 mSec.

y_9 8.13 mSec.

y_{10} 16.26 mSec.

Vertical Blanking

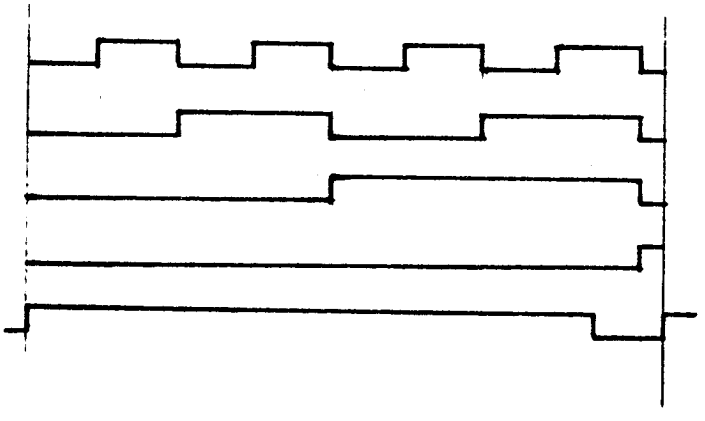
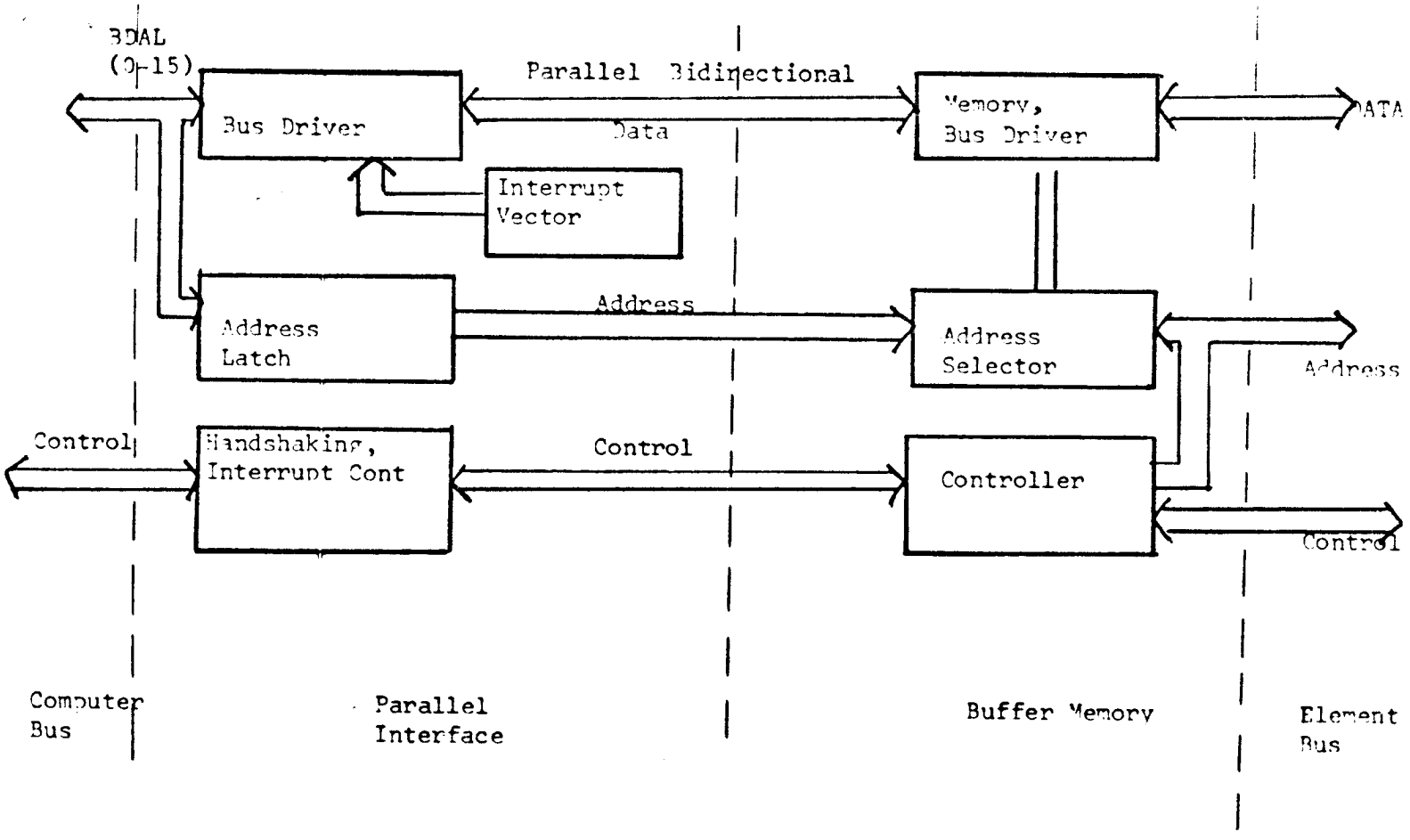


Figure 2


BDAL
(0-15)
Bus Driver
Parallel Bidirectional
Data
Memory,
Bus Driver
DATA
Interrupt
Vector
Address
Latch
Address
Address
Selector
Address
Control
Handshaking,
Interrupt Cont
Control
Controller
Control
Computer
Bus
Parallel
Interface
Buffer Memory
Element
Bus

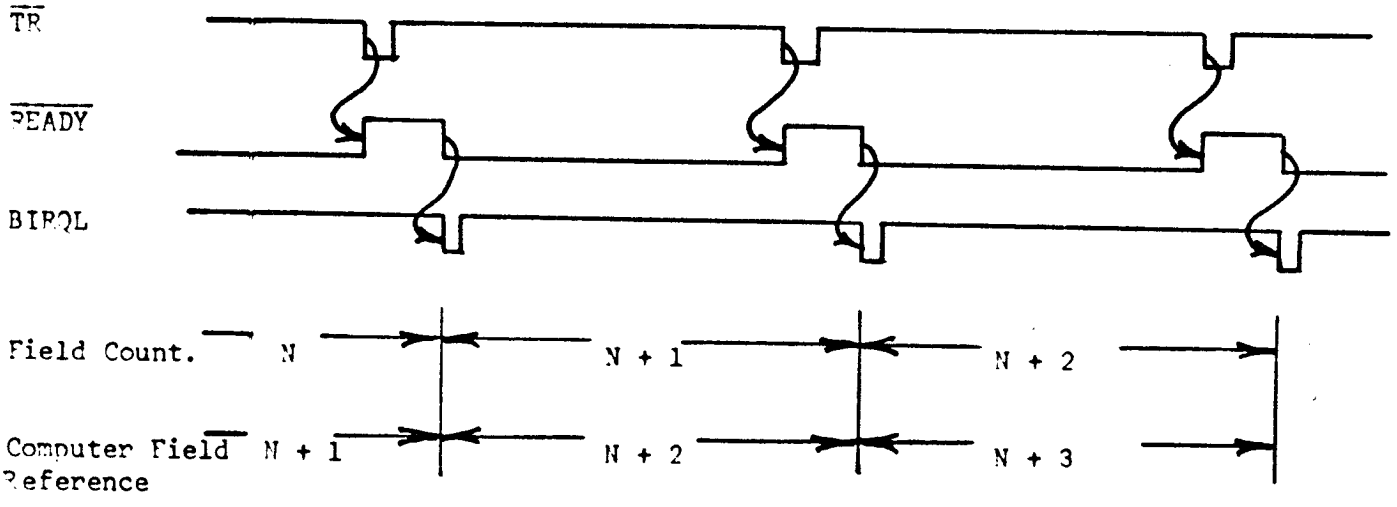

TR
READY
BIRQL
Field Count.
N
N + 1
N + 2
Computer Field
Reference
N + 1
N + 2
N + 3

Figure 3

Element Bus

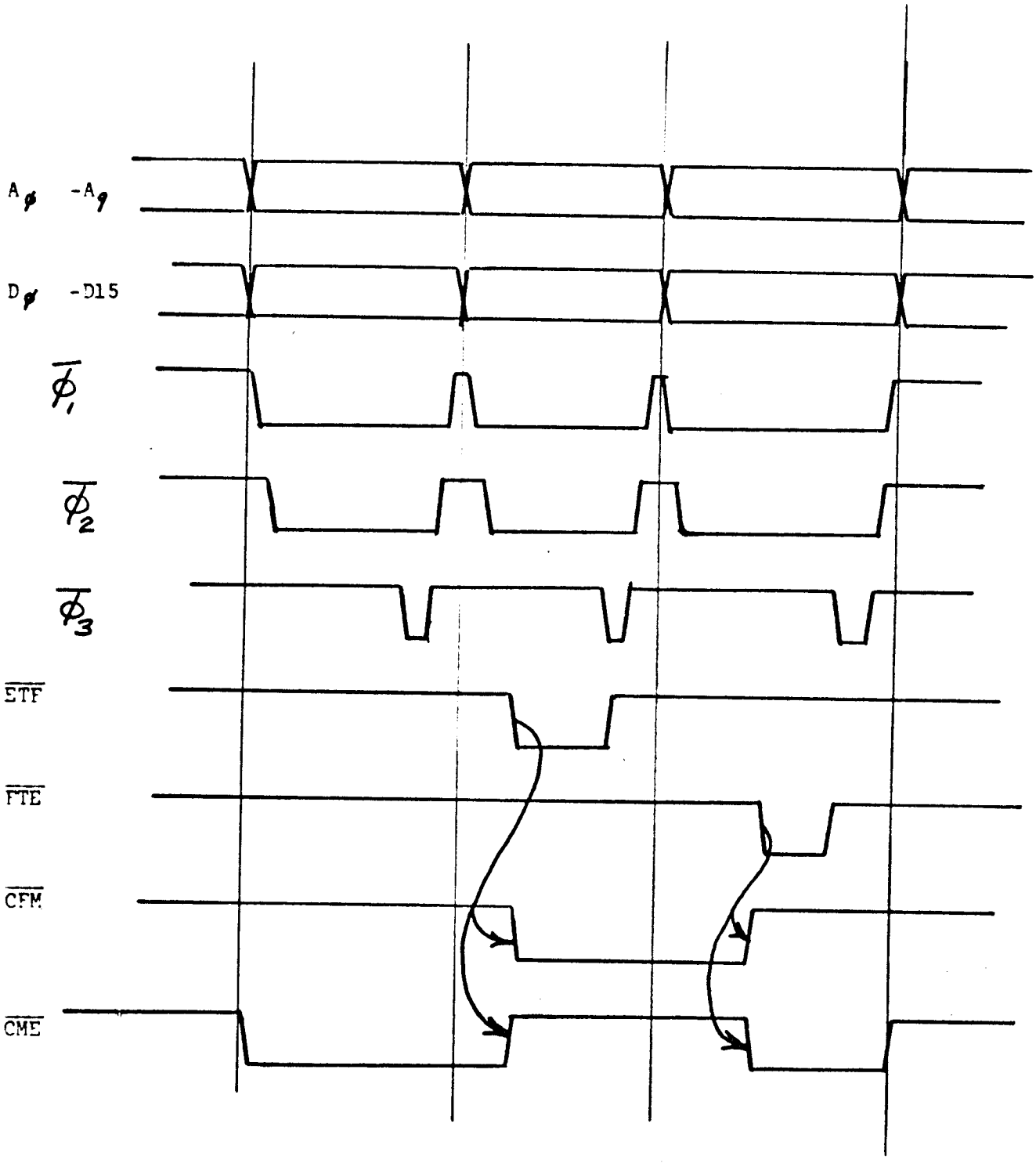


Figure 4

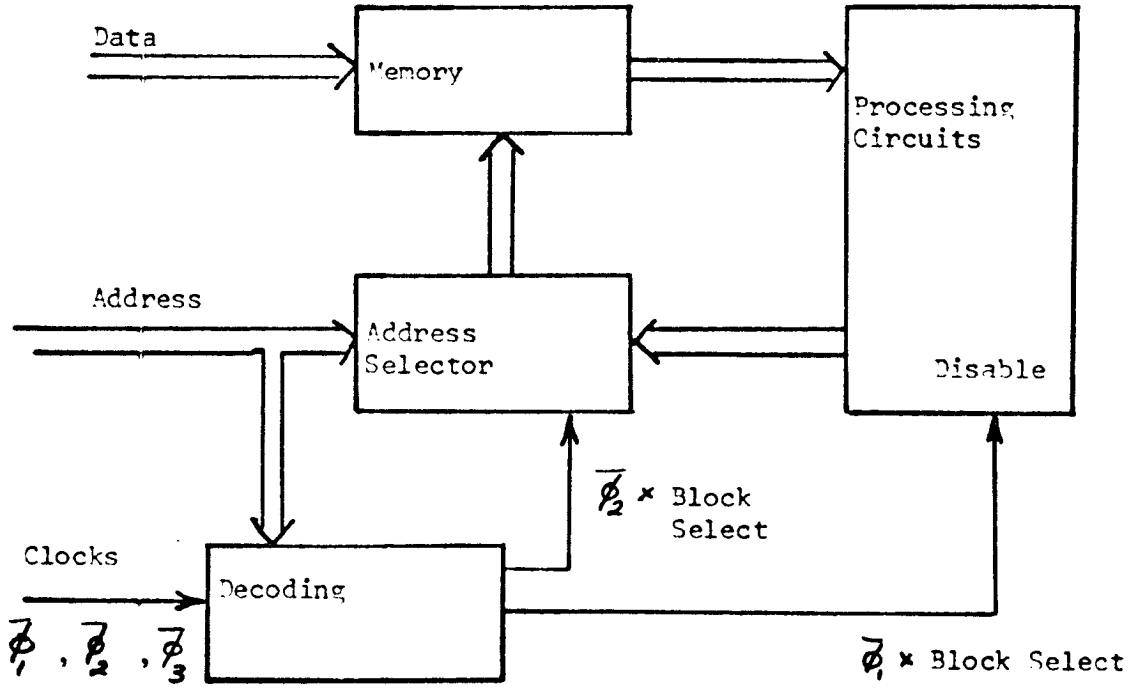

Data
Memory
Processing
Circuits
Address
Address
Selector
Disable
$\overline{\phi_2}$ × Block
Select
Clocks
Decoding
$\overline{\phi_1}$, $\overline{\phi_2}$, $\overline{\phi_3}$
$\overline{\phi_1}$ × Block Select

Figure 5